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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/606,715	06/26/2003	Benjamin Thomas Percer	200312936-1	5780

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EXAMINER	
LE, JOHN H	

ART UNIT	PAPER NUMBER
2863	

DATE MAILED: 11/15/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/606,715	PERCER ET AL.	
	Examiner	Art Unit	
	John H Le	2863	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8,13,16 and 18-24* is/are rejected.

7)☒ Claim(s) *9-12,14,15 and 17* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 June 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *06/26/2003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claims 7, 18, 20, 21, and 23 are objected to because of the following informalities:

Claim 7, line 3, after "generating", "an fault signal" should change to –a fault signal--.

Claim 18, line 2, after "BMC", insert –(Baseboard Management Controller)--.

Claim 20, line 1, after "I^2C-based bus", insert –(Inter-Integrated Circuit)--.

Claim 21, line 1, after "IPMP", insert –(Intelligent Platform Management Bus)--.

Claim 23, line 1, after "BMC", insert –(Baseboard Management Controller)--.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1-4, 6-8, 13, 16, 22 are rejected under 35 U.S.C. 102(e) as being anticipated by Matsushige (US 2003/0101020 A1).

Regarding claim 1, Matsushige discloses a system for margin testing one or more components of the computer system (Abstract), comprising a fault bypass module (port bypass circuit) incorporated in said electronic system, said fault bypass module masking signals indicative of faults associated with one or more of said components during margin testing of said electronic system ([0143]-[0145]).

Regarding claim 2, Matsushige discloses at least one of said faults corresponds to an operating parameter associated with at least one of said components crossing a selected threshold ([0057]-[0061], [0128]).

Regarding claim 3, Matsushige discloses said operating parameter is any of voltage ([0066]).

Regarding claim 4, Matsushige discloses a controller (15) internal to said electronic system and in communication with said fault bypass module, said controller transmitting a command to said fault bypass module for initiating masking of said fault signals by said module ([0055]-[0057], [0062]).

Regarding claim 6, Matsushige discloses said fault bypass module permits normal processing of said fault signals during normal operation of said electronic system ([0100]).

Regarding claim 7, Matsushige discloses a hardware monitor (micro processor 15) in communication with said controller and with at least one of said

components, said hardware generating a fault signal in response to occurrence of a fault associated with said at least one component ([0088]-[0091]).

Regarding claim 8, Matsushige discloses said hardware monitor transmits said fault signal to said fault bypass module, said fault bypass module masking said received fault signal during margin testing of said electronic device ([0088]).

Regarding claim 13, Matsushige discloses a programmable logic device programmed to provide masking of said fault signals (0141]).

Regarding claim 16, Matsushige discloses said electronic system comprises a computer system ([0066]).

Regarding claim 22, Matsushige discloses a system for margin testing one or more components of the computer system (Abstract), comprising: a fault bypass module (port bypass circuit) incorporated in said electronic system, said fault bypass module masking signals indicative of faults associated with one or more of said components during margin testing of said electronic system ([0143]-[0145]), an internal controller (15) in communication with said fault bypass module for transmitting a command to said fault bypass module to initiate masking of said fault signals by said module ([0055]-[0057], [0062]).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Matsushige (US 2003/0101020 A1) in view of Choudhury et al. (USP 6,725,404).

Regarding claim 5, Matsushige fails to disclose said fault signals comprise: interrupt signals.

Choudhury et al. disclose said fault signals (Col.6, lines 10-22) comprise: interrupt signals (e.g. Col.4, lines 25-42).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to include interrupt signals as taught by Choudhury et al. in a margin test method of Matsushige for the purpose of providing a test apparatus and method of determining the reliability and/or suitability of an electrical connector for use at a desired data rate by sensing a propagation delay imposed by the electrical connector on a test signal (Choudhury et al., Col.2, lines 30-35).

6. Claim 18-21 and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Matsushige (US 2003/0101020 A1) in view of Hawkins et al. (US 2003/0130969 A1).

Regarding claims 18-21 and 23, Matsushige fails to disclose a controller comprises a Baseboard Management Controller (BMC), wherein said communication bus is an Inter-Integrated Circuit bus (I^2C bus), wherein said I^2C bus is Intelligent Platform Management Bus (IPMB).

Hawkins et al. disclose a controller comprises a Baseboard Management Controller (BMC) ([0015]-[0017]), wherein said communication bus is an Inter-Integrated Circuit bus (I^2C bus)([0006]), wherein said I^2C bus is IPMB ([0013]).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to include a Baseboard Management Controller (BMC), an Inter-Integrated Circuit bus (I^2C bus), wherein said I^2C bus is Intelligent Platform Management Bus (IPMB) as taught by Hawkins et al. in a margin test method of Matsushige for the purpose of providing a star Intelligent Platform Management Bus Topology.

7. Claim 24 is rejected under 35 U.S.C. 103(a) as being unpatentable over Matsushige (US 2003/0101020 A1) in view of Templeton et al. (USP 6,667,917).

Regarding claim 24, Matsushige disclose intercepting one or more signals indicative of faults associated with one or more components of said electronic system during margin testing thereof ([0143]-[0145]).

Matsushige fails to disclose masking said intercepted signals by generating signals indicative of absence of said faults.

Templeton et al. disclose masking said intercepted signals by generating signals indicative of absence of said faults (e.g. a pass result can indicate that there are no faulty, Col.7, lines 36-40).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to inform generating signals indicative of absence of said faults as taught by Templeton et al. in a margin test method of Matsushige for the purpose of providing a method for identification of faulty or weak functional logic elements under simulated extreme operating conditions.

Allowable Subject Matter

8. Claims 9-12, 14-15, and 17 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter:

Regarding claim 9, none of the prior art of record teaches or suggests the combination of a system for margin testing one or more components of the computer system, wherein the system comprising a fault bypass module incorporated in said electronic system, said fault bypass module masking signals indicative of faults associated with one or more of said components during margin testing of said electronic system; and a power control element in communication with said fault bypass module, said fault bypass module transmitting one of more of said fault signals to said power control element in absence of margin testing and masking said one or more fault signals during margin testing of said electronic system.

Regarding claim 11, none of the prior art of record teaches or suggests the combination of a system for margin testing one or more components of the computer system, wherein the system comprising a fault bypass module incorporated in said electronic system, said fault bypass module masking signals indicative of faults associated with one or more of said components during margin testing of said electronic system; a controller internal to said electronic system and in communication with said fault bypass module, said controller transmitting a command to said fault bypass module for initiating masking of said

fault signals by said module; and a hardware monitor in communication with said controller and with at least one of said components, said hardware generating an fault signal in response to occurrence of a fault associated with said at least one component, wherein said at least one component is a power rail, and said hardware monitor generates an interrupt signal in response to a voltage associated with said power rail varying from a nominal value by more than a selected threshold. It is these limitations as they are claimed in the combination with other limitations of claim, which have not been found, taught or suggested in the prior art of record, that make these claims allowable over the prior art.

Regarding claim 14, none of the prior art of record teaches or suggests the combination of a system for margin testing one or more components of the computer system, wherein the system comprising a fault bypass module incorporated in said electronic system, said fault bypass module masking signals indicative of faults associated with one or more of said components during margin testing of said electronic system; a controller internal to said electronic system and in communication with said fault bypass module, said controller transmitting a command to said fault bypass module for initiating masking of said fault signals by said module; a hardware monitor in communication with said controller and with at least one of said components, said hardware generating an fault signal in response to occurrence of a fault associated with said at least one component; and temperature diode coupled to at least one of said components and said hardware monitor for measuring a temperature of said component and supplying said measured temperature to said hardware monitor. It is these

limitations as they are claimed in the combination with other limitations of claim, which have not been found, taught or suggested in the prior art of record, that make these claims allowable over the prior art.

Regarding claim 15, none of the prior art of record teaches or suggests the combination of a system for margin testing one or more components of the computer system, wherein the system comprising a fault bypass module incorporated in said electronic system, said fault bypass module masking signals indicative of faults associated with one or more of said components during margin testing of said electronic system; a controller internal to said electronic system and in communication with said fault bypass module, said controller transmitting a command to said fault bypass module for initiating masking of said fault signals by said module; and a hardware monitor in communication with said controller and with at least one of said components, said hardware generating an fault signal in response to occurrence of a fault associated with said at least one component, wherein said fault bypass module intercepts a selected output signal of said at least one component and generates a simulated signal corresponding to said intercepted output signal for transmittal to said hardware monitor during margin testing of said component. It is these limitations as they are claimed in the combination with other limitations of claim, which have not been found, taught or suggested in the prior art of record, that make these claims allowable over the prior art.

Regarding claim 19, none of the prior art of record teaches or suggests the combination of a system for margin testing one or more components of the

computer system, wherein the system comprising a fault bypass module incorporated in said electronic system, said fault bypass module masking signals indicative of faults associated with one or more of said components during margin testing of said electronic system; a controller internal to said electronic system and in communication with said fault bypass module, said controller transmitting a command to said fault bypass module for initiating masking of said fault signals by said module, wherein said controller comprises a Baseboard Management Controller (BMC); and a communication bus for providing communication between said BMC and said fault bypass module. It is these limitations as they are claimed in the combination with other limitations of claim, which have not been found, taught or suggested in the prior art of record, that make these claims allowable over the prior art.

Contact Information

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to John H Le whose telephone number is 571-272-2275. The examiner can normally be reached on 8:00 - 4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John E Barlow can be reached on 571-272-2269. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

John H. Le

Patent Examiner-Group 2863

November 9, 2004

John Barlow
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